Abstract of the Disclosure

In an arithmetic device which performs a multiplication of a multiplicand A and a multiplier B expressed by bit patterns using a secondary Booth algorithm, an encoder selects a partial product indicating -A when the value of i specifying three consecutive bits of B is 0, and selects a partial product indicating 0 when the value of i is not 0. An addition circuit generates a two's complement of A from the partial product indicating -A, and outputs it as a multiplication result.